





## MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

Sponsored by CMR Educational Society

(Affiliated to JNTU, Hyderabad, Approved by AICTE - Accredited by NBA & NAAC - "A" Grade - ISO 9001:2015 Certified) Maisammaguda, Dhulapally (Post Via Hakimpet), Secunderabad – 500100, Telangana State, India. Contact Number: 040-23792146/64634237, E-Mail ID: <u>mrcet2004@gmail.com</u>, website: <u>www.mrcet.ac.in</u>

## DEPARTMENT OF INFORMATION TECHNOLOGY II B.TECH I SEMESTER R17 SUPPLEMENTARY PREVIOUS QUESTION PAPERS



# LIST OF SUBJECTS

CODE	NAME OF THE SUBJECT
R17A0510	Computer Organization
R17A0461	Digital Logic Design
R17A0504	Data Structures using C++
R17A0401	Electronic Devices and Circuits
R17A0503	Mathematical Foundation of Computer Science
R17A0024	Probability and Statistics

#### Code No: R17A0510 MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY (Autonomous Institution – UGC, Govt. of India) II B.Tech I Semester Supplementary Examinations, February 2021 Computer Organization

				<b>-</b> -	(CSE	& I	<b>T</b> )		_						
			Roll No												
Tin	ne: 2	2 hours 30	min								Μ	[ax.]	] Mai	rks: 7	70
				Answer	Any l	Five	Ques	tion	s						
			All	Questio	ons cai	rries **	equa	l ma	rks.						
1	a)	Explain va	arious number sys	tems an	d num	ber 1	epre	senta	ation	s use	ed in	syst	em.		[7M]
	b	) Dividend	A=01110 Divisor	B=100	01. Ex	plair	n flov	vcha	rt fo	r divi	ide o	pera	ntior	1.	[7 <b>M</b> ]
2	a)	Convert th	ne $(256)_{10}$ into foll	owing c	codes										[7M]
		i) Bir	nary Coded Decim	al (BCI	<b>D</b> )		ii	) Ex	cess	3 co	des				[7M]
		iii) G	ray code				i	v) Re	eflec	ted (	Code	:			
	b	) Explain a	ddition and subtra	ction al	gorith	ms f	or da	ta re	pres	entec	d in s	signe	ed		
	m	agnitude a	nd signed 2's com	pliment	•										
3	a)	What are th	he different phases a	a basic c	omput	er ins	tructi	on cy	ycle d	consi	sts? I	Expla	iin		[7M]
		instruction	cycle with flowcha	rt.											[7M]
	b)	a) Explain	the design of contro	ol unit. H	low to	deco	de the	e mic	ro op	oerati	on fi	elds?	'Exj	plain	
		the process	8.												
4	a)	Write the f	format of the micro	instructio	on and	micr	o ope	ratio	ns fo	r the	cont	rol m	iema	ory.	[7M]
	b)	With neat s	sketch explain the d	esign of	contro	l unit	of ba	asic c	comp	uter.					[/ייין
5	a)	What are the	he different types of	address	ing mo	odes a	and ex	xplai	n wit	h exa	mple	es			[7M] [7M]
	b)	Write the n	nultiplication algori	thm and	explai	n wit	h an o	exam	ple						[/ייין
6	a)	Draw the c	Fircuit for 4-Bit BCI	O Adder	and ex	plain	its o	perat	ions.						[7M] [7M]
	b)	Explain the	e STACK Organizat	tion											[,]
7	a)	Differenti	ate parallel proces	sing and	d pipe	line j	proce	essin	g and	d exp	olain	ther	n.		[7M] [7M]
	b)	Explain a	rithmetic pipeline	with exa	ample										[,]
8	a)	What is vi	irtual memory? W	ith the l	nelp of	fneat	t sket	ch e	xpla	in th	e me	thod	l of		[7M] [7M]
	vi	irtual to phy	ysical address tran	slation.											[/171]
	b	) Explain th	ne READ and WR	ITE ope	eration	is in .	Asso	ciati	ve M	lemo	ory				

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### Code No: R17A0461 MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY (Autonomous Institution – UGC, Govt. of India) II B.Tech I Semester Supplementary Examinations, February 2021 Digital Logic Design

				( <b>I</b>	<b>T</b> )								
		Roll No											
Time:	2 hours 30	) min								N	lax.	Mark	s: 70
			Answer A	Any I	Tive	Ques	tion	S					
		All	l Questio	ns cai	rries	equa	l ma	rks.					
				*:	**								
1	a) Perform	m the arithmetic	operation	n usir	ng 1s	and	2s c	comp	leme	ent si	ubtra	action (	of <b>[8M]</b>
	(54) <sub>10</sub> fro	m (231) <sub>10</sub>	-		-			_					
	b) What do you mean by error correcting code. Write briefly about hamming code.										e. [6M]		
2	a)Draw the circuit diagram of $((AB)'(CD)')'$ using AND, OR, NOT gates and then [										en <b>[8M]</b>		
	Realize the expression using NAND gates only.												
	b) Prove	the Boolean expr	ession	•		•							
	XYZ + X	XYZ' + XY'Z + X'	Y'Z + X'Y	Z' =	Y'Z	+XY	y' + X	X'YZ'					[6M]
3	a) Simpli	fy using K-map	i) XY +	-WXY	Z' +	-X'Y	i	i) X'	+ Y'	+X	YZ'		[6M]
	b) Draw the multi-level NOR circuit for the following expression									on <b>[8M]</b>			
	w = (x + y +	z)+xyz								U		1	
4	Minimiz	e the expression	F(a,b,c,d	) = (1)	1,3,5.	7,14	,15)-	+ d(9	9,11)	us	ing t	the inp	ut <b>[14M]</b>
	NOR gate	es implementation	n of the n	ninim	ized	func	tion				U	1	
	0	1											
5	a) Explain	n about 3 to 8 dec	coder usi	ng its	blac	k dia	gran	n and	l log	ic dia	agrai	m.	[ <b>8M</b> ]
	b) Design	a BCD to Exces	s-3 code	conv	erter		U		U		U		[6M]
6	a)Draw th	he block diagram	of a 4-bi	t para	llel a	ıddeı	: & e	xpla	in its	ope	ratio	on.	[8M]
	b) Distinguish between decoder and an encoder with relevant example										[6M]		
7	a) Compa	rison between Co	ombinatio	onal a	and S	eaue	ntial	l logi	ic cir	cuits			[8M]
	b) Draw the characteristic table of IK Flip Flop and obtain its characteristic										ic [6M]		
	equation.				1		L						
8	a)Give th	e PLA realization	n of the fo	ollow	ing F	Funct	ions						[ <b>8M</b> ]
-	F	$1 = \sum m (0.1.3.5.)$	7.8.9.11.	13.14	)	F2 =	= Σ n	n (1.	3.5.7	.9.11	.13.	.15)	L1
	b) Write the	he differences betw	veen RON	1. PAI	L and	PLA		( )	<i>j- j</i> •	<i></i>	, - ,		[6M]
	- /		*	****	****	*							[]

**R17** 

#### Code No: **R17A0504** MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY (Autonomous Institution – UGC, Govt. of India) **II B.Tech I Semester Supplementary Examinations, February 2021 Data Structures using C++** (CSE & IT) **Roll No** Time: 2 hours 30 min Max. Marks: 70 Answer Any Five Questions All Questions carries equal marks. \*\*\* 1 a) Explain & Differentiate between time and space complexity [7M] b) Explain binary search with the help of a Program. [7M] 2 Form and solve the recurrence relation for the running time of factorial (a) [7M] method and hence determine its big-O complexity long factorial (int n) { if (n == 0)return 1; else return n \* factorial (n-1); Sort the sequence 3, 1, 4, 1, 5, 9, 2, 6, 5 using insertion sort. Analyse the [7M] (b) running time of Insertion Sort, if the input is sorted 3 (a) Develop PUSH() and POP() routines of stack-linked implementation [7M] Perform following operations on stack using linked list with the assumption of top=NULL, (push(3) push(6) push(2) pop() push(7) push(1)). (b). write an algorithm to convert an expression from infix to postfix notation. Convert ( (A + B) \* C – (D - E)) ^ (F + G) to postfix expression [7M] a). Explain how to insert and delete elements in a circular linked list with 4 [7M] an example b).Develop routines insert(), delete() for queue using linked list [7M] implementation. 5 Examine about any one External Sorting Model with an example [14M] [14M]

- Explain minimum and maximum heap with example. 6
- Explain different collision resolution techniques in data structures. 7 [14M] 8 Define the Graph. Explain the BFS and DFS algorithms with an example [14M]

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# Code No: R17A0401 R17 MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY (Autonomous Institution – UGC, Govt. of India) II B.Tech I Semester Supplementary Examinations, February 2021 Electronic Devices and Circuits (EEE ECE CSE & IT)

	Roll No										
Time:	2 hours 30 min Max. Marks: 7	<b>'</b> 0									
	Answer Any <b>Five</b> Questions										
	All Questions carries equal marks. ***										
1	a) Illustrate different equivalent circuits of a Diode.	[6M]									
	b) What are the different breakdown mechanisms occur in semiconductor diodes?	[8M]									
	Explain them.										
2	a) Describe the principle of operation and characteristics of Tunnel with the help	[8M]									
	of neat diagrams.										
	b) Explain the principle of operation and characteristics of a Varactor Diode.										
3	a) Draw the Full wave Rectifier circuit and then explain its operation with a neat	[5M]									
	equivalent circuits and waveforms.	[9M]									
	b) Derive the expressions of Vavg, Vrms, Ripple factor, Conversion Efficiency										
	and PIV for Bridge Rectifier without filter.										
4	a) With mathematical expressions, discuss different harmonic components	[6M]									
	present at the output of rectifier.	[8M]									
	b) Design Centre-tapped full-wave rectifier circuit using capacitor filter and then										
	derive its ripple factor expression.										
5	a) Describe the construction and operation of BJT.	[6M]									
	b) Draw and explain the input and output characteristics of common emitter	[8M]									
	configuration.										
6	By analysing single-stage CE amplifier using h-parameter model derive the	[14M]									
	expressions of current gain, voltage gain, input impedance and output impedance.										
7	Draw the self bias circuit with BJT and derive expressions for all the three stability	[14M]									
	factors.										
8	a) Discuss the construction and operation of n-channel JFET.	[8M]									
	b) Draw and explain the drain and transfer characteristics of JFET.	[6M]									

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#### Code No: R17A0503 MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY (Autonomous Institution – UGC, Govt. of India) **II B.Tech I Semester Supplementary Examinations, February 2021 Mathematical Foundation of Computer Science** (CSE & IT) **Roll No** Time: 2 hours 30 min Max. Marks: 70 Answer Any Five Questions All Questions carries equal marks. \*\*\*\* a) Identify whether the following sentences are propositions or not. If proposition, 1 [7M] write its truth value. (i) 2+3=5. (ii) 5+7=10. (iii) x + 2 = 11(iv) Answer this question. (vi) What time is it? (v) Do not pass go. (vii) Read this carefully. (viii) $2n \ge 100$ . b) Construct truth tables for the following: [**7M**] (i) $(p \lor q) \land r$ (ii) $(p \lor \neg q) \rightarrow r$ (iii) $(p \downarrow q) \land (p \downarrow r)$ 2 a) Identify whether the following Inference is valid or Invalid. If Invalid, state the [5M] fallacy CVD (C VD)→~H $\sim H \rightarrow (A^{\wedge} \sim B)$ $(A \land \neg B) \rightarrow (R \lor S)$ R V S [**9**M] b) Prove that the following are equivalent (i) $p \lor (\sim p \land q) \equiv (p \lor q)$ (ii) $\mathbf{p} \wedge (\sim \mathbf{p} \lor \mathbf{q}) \equiv (\mathbf{p} \land \mathbf{q})$ 3 a) Consider the relation $R = \{(a,a), (b,b), (c, c), (d,d), (a,b), (b,a)\}$ on set $A = \{a,b,c,d\}$ [7M] }. Predict whether R is reflexive or Symmetric or Transitive? If any property does not satisfy, state the reason. [**7**M] b)

Which of the following graphs are isomorphic?



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- a) Let  $a=\{1,2,3,4,5\}$  and  $R=\{(1,1), (1,3), (1,4), (1,5), (1,1), (2,2), (2,3), (2,4), (2,5), (3,3), (3,4), (3,5), (4,4), (5,5)\}$  Show that the relation R is a partial order and draw its hasse diasgram
  - b) When R is called a Equivalence relation, what are the conditions and give an [7M] example for the relation
- 5 a)In how many ways can the letters be arranged so that all the vowels come together? [7M] Word is "IMPOSSIBLE."

b)In how many ways of 4 girls and 7 boys, can be chosen out of 10 girls and 12 boys to make the team?

6 (a)From a group of 8 women and 6 men, a committee consisting of 3 men and 3 women [7M] is to be formed. In how many ways can the committee be formed if two of the women refuses to serve together

(b) How many words with or without meaning, can be formed by using all the letters **[7M]** of the word 'AMARAVATHI' using each letter exactly once?

7 Solve the recurrence relation

4

[14M]

[**7**M]

8 Explain Kruskal's Algorithm in detail and mention how minimum spanning tree for the [14M] following graph G for the below diagram



### **Code No: R17A0024** MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY (Autonomous Institution – UGC, Govt. of India) **II B.Tech I Semester Supplementary Examinations, February 2021**

**Probability and Statistics** 

-		
(CSE	&	IT)

		Roll	No								
Time	2 hours 30	) min							Max.	Marks:	70
				Answe	r Any <b>F</b>	<b>ive</b> Que	stions				
			Al	l Quest	ions car	ries equa	al marks	•			
					**:	**					
1	A random	variable	X has t	the follo	owing pr	obabilit	y distrib	ution			[14M]
	Value of	f 0	1	2	3	4	5	6	7	8	
	Х										
	P(x)	0	3a	5a	7a	9a	11a	13a	15a	17a	
	(i)	Determi	ine the	value of	f a	(ii) Fin	d p(x < 3)	) (iii) Fi	nd p(x>	-3)	
	(iv) Fi	nd the dis	stributi	on func	tion F(x)	)					
2	20% of ite	ems produ	uced fro	om a fac	ctory are	defectiv	ve. Find	the prob	ability	that in a	[14M]
	sample of	5 chosen	at rand	lom							
	(i)	None is	s defec	tive (i	i) one i	s defect	ive (iii	i) p(1 <x< td=""><td>(iv</td><td>y) Mean</td><td></td></x<>	(iv	y) Mean	
		(v) Vari	ance								
3	Find the K	Karl Pears	son's co	oefficier	nt of cor	relation	from the	follow	ing data	l	[14M]
	Ween	va   10	101	102	102	100	00	07 0		05	

Wages 100 101 100 98 96 102 102 91 95 Cost of 98 99 99 97 95 92 95 94 90 91 living

4 Price indices of cotton and wool are given below for the 12 months of a year. [14M] Obtain the equations of lines of regression between indices.

Price	78	77	85	88	87	82	81	77	76	83	97	93
index of												
cotton(X)												
Price	84	82	82	85	89	90	88	92	83	89	98	99
index of												
wool (Y)												

- In sample of 1000 people in Karnataka 540 are rice eaters and the rest are wheat 5 [14M] eaters. Can we assume that both rice eaters and wheat eaters are equally popular in this state of Karnataka.
- 6 A random sample of size 64 is taken from a normal population with mean 51.4 [14M] and variance 68. What is the probability that the mean of the sample will (i) exceed 52.9 (ii) fall between 50.5 and 52.3 (iii) be less than 50.6
- 7 A random sample from a company's very extensive files shows that the orders for [14M] a certain kind of machinery were filled, respectively in 10,12,19,14,15,18,11 and 13 days. Use the level of significance 0.01 to test the claim that on the average such orders are filled in 10.5 days. Choose the alternative hypothesis so that



rejection of null hypothesis  $\mu = 10.5$  days implies that it takes longer than indicated.

- 8 A bank plans to open a single server drive-in banking facility at a certain centre. [14M] It is estimated that 20 customers will arrive each hour on average. If on average, it requires 2 minutes to process a customer's transaction, determine
  - (i) The proportion of time that the system will be idle,
  - (ii) On the average , how long a customer will have to wait before reaching the server,
  - (iii) The fraction of customers who will have to wait.

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